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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,860	03/21/2000	Jorge Humberto Figueredo	041-481-RB	6689

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EXAMINER
WEST, JEFFREY R

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,860	FIGUEREDO, JORGE HUMBERTO	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawing in Figure 2A is objected to as failing to comply with 37 CFR 1.84(p)(5) because it includes the following reference sign(s) not mentioned in the description: "29ex". A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawing in Figure 2B is objected to because of the following informalities:

In Figure 2B, component "39" should be labeled "39a" to be in accordance with page 10, line 18. Also, it is unclear why the top epoxy sections of components "39a" and "49a" are both labeled "29x" while the bottom epoxy sections of components "39a" and "49a" are labeled "39x" and "49x" respectively.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

On page 6, lines 31-35, Applicant describes flow charts present in Figures 6A and 6B, however, Figures 6A and 6B are not present in the instant invention.

Further descriptions of nonexistent Figures 6A and 6B are present on page 15, lines 24+.

On page 10, line 33, "29a, 39 and 49" should be ---29a, 39a and 49a--- to be in accordance with Figure 2B and the previous description on page 10, lines 18-19.

On page 12, lines 12-13, "test that circuit 30 connected" should be ---test socket 30 connected---.

On page 18, line 6, Applicant describes 5A as showing "step N", while Figure 5A displays a graph without any associated steps.

Appropriate correction is required.

Claim Objections

4. Claims 1 and 5 are objected to because of the following informalities:

In claim 1, the language "incrementally reducing" is unclear. It is suggested that Applicant change "incrementally reducing" to ---reducing--- or change the wording to language similar to that of subsequent claims such as ---sequentially reducing---.

In claim 5, "wherein step B" should be ---wherein step (b)---.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,938,410 to Kondo in view of JP Patent No. 10-239373 to Agawa and further in view of U.S. Patent No. 4,739,258 to Schwarz and U.S. Patent No. 5,844,330 to Furukawa et al.

Kondo discloses a soldering apparatus of a reflow type in which electric parts, such as chips, temporarily mounted on a printed circuit board are soldered with solder preforms or solder pastes (column 1, lines 5-10). Kondo also teaches a common method for testing the adherence of the solder plates to the printed circuit board by rapidly heating and thereafter rapidly cooling (i.e. temperature ramping) the device under test in order to inspect the solder connections for air bubbles or solder scattering which causes short circuiting of the wiring (column 2, lines 37-57).

While Kondo does suggest that, during testing, solder scattering causes short circuiting, Kondo does not teach a method for determining whether or not short circuiting has occurred, specifically by plotting a graph of the power bus to ground resistance of the device. Kondo also doesn't specify that the temperature ramping start and end at room temperature.

Agawa teaches a short circuit checker used in packaging parts of printed circuit boards comprising attaching the printed circuit base to a test socket (0007) and monitoring the resistance between the power supply line (i.e. power bus) and common line (i.e. ground) in order to determine the occurrence of a short circuited,

faulty component (0004) which is indicated by a non-linear, rapid change in resistance (0009).

Schwarz teaches a method for the dynamic testing of thin-film conductors comprising placing a semiconductor wafer on a test platform or stage of a test unit (i.e. socket), ramping a current to a resistive heating element in order to linearly increase the heat of the conductor (column 2, line 67 to column 3, line 14), and measuring the voltage and current to calculate and plot the change in resistance over temperature of the conductor (column 5, lines 53-64) wherein the plot characteristics are analyzed in order to determine a failure condition (column 3, lines 14-20).

It would have been obvious to one having ordinary skill in the art to modify the invention of Kondo to include monitoring the change in power bus to ground resistance, as taught by Agawa, because Agawa suggests a method that would be applicable in the invention of Kondo to determine when a change in temperature has caused a short circuit due to solder scattering in a quick, accurate, and non-destructive way (0011).

It would have been obvious to one having ordinary skill in the art to modify the invention of Kondo and Agawa to include plotting a graph to determine a failure condition, as taught by Schwarz, because Schwarz suggests a well known method of plotting the changing characteristics of a value to produce clear, easily discernable results regarding the changes, as would be applicable in displaying a rapid change in resistance taught by the invention of Kondo and Agawa.

Also, although the invention of Kondo, Agawa, and Schwarz doesn't specifically disclose starting and ending the temperature ramping at room temperature, the invention of Kondo, Agawa, and Schwarz does disclose determining the effect of solder scatter due to melting and/or expansion of the solder while the invention of Furukawa teaches the changing properties of solder with respect to temperature, specifically that solder is solid at room temperature (column 6, lines 44-57). Therefore in order to examine the effects of solder scatter/expansion, it would have been obvious to one having ordinary skill in the art to monitor the solder as it changes from solid to liquid form (i.e. to and from room temperature).

Further, although not specifically disclosed, it is considered inherent that in order for the resistance to be monitored over time, the measuring devices must obtain the data at some selected interval and, with respect to claim 7, since Applicant fails to provide the criticality of increasing and decreasing the temperature 20 degrees and only describes adjusting the temperature from 20 to 30 degrees to test any non-linearity of the resistance (page 11, lines 16-23 and page 14, lines 14-17), this feature is considered to be an engineering design choice with the invention of Kondo, Agawa, Schwarz, Furukawa teaching a functionally equivalent method.

7. Claims 5, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Agawa, Schwarz, and Furukawa and further in view of U.S. Patent No. 5,419,780 to Suski.

As noted above, Kondo in combination with Agawa, Schwarz, and Furukawa teaches many of the features of the claimed invention including heating and cooling a component under test in order to determine short circuiting conditions but does not teach a corresponding device to implement the cooling operation.

Suski teaches a method and apparatus for recovering power from a semiconductor circuit using a well known Peltier-junction thermoelectric heat-reducing cooler which generates a temperature differential between two opposing surfaces (i.e. temperature transfer blocks) (column 4, lines 59-62) wherein one of the surfaces is conductively, such as with a metallic shield or adhesive (column 4, lines 5-8), connected to the surface of the device under test (column 5, lines 27-34). Suski also teaches connecting the Peltier device to a heat sink and corresponding fan (Figure 5), and while Suski teaches an embodiment without a computer controlled power supply for powering the fan, Suski does teach a functionally equivalent method applicable when the fan doesn't require a large amount of power (column 5, lines 56-52) and also teaches other well known systems that do implement controlled fan power supplies if power constraints allow it (column 4, lines 23-36).

It would have been obvious to one having ordinary skill in the art to modify the invention of Kondo, Agawa, Schwarz, and Furukawa to include the specifics of a component to cool the device under test, a taught by Suski, because Suski suggests a device necessary to accurately carry out the cooling in the invention of Kondo,

Agawa, Schwarz, and Furukawa using device common for semiconductor applications (column 2, lines 3-8 and column 4, lines 57-62).

Although the invention of Kondo Agawa, Schwarz, Furukawa, and Suski doesn't specifically disclose attaching a digital multi-meter to the test socket in order to measure the power-bus to ground resistance, the invention of Kondo Agawa, Schwarz, Furukawa, and Suski does teach including a probe attached to the test socket to measure the resistance (Agawa, 0005) and it would have been obvious to one having ordinary skill in the art to specify that the measuring be implemented using a digital multi-meter because digital multi-meters are devices very well known in the art for accurately measuring resistance. Similarly it would have been obvious to one having ordinary skill in the art to use a computer program to apply the necessary current to activate the heater because a computer program would provide greater control in the heating range therefore reduced the occurrence of damage to the component under test due to extreme temperatures.

With respect to claims 6 and 9, Applicant fails to provide the criticality for specifying that the measurements be logged every two seconds (page 18, lines 11-18) and therefore this features is also considered an engineering design choice. Further, it is well known in the art that the accuracy of resulting measurements improve as more data samples are taken the therefore it would have been obvious to one having ordinary skill in the art to take measurements at any interval that produces the desired accuracy.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 5,260,668 to Mallory et al. teaches a semiconductor surface resistivity probe including control of the temperature over a predetermined range to obtain a plot of resistivity as a function of temperature.

U.S. Patent No. 6,226,994 to Yamada et al. teaches a thermoelectric element and thermoelectric cooling or heating device such as a Peltier element.

U.S. Patent No. Re. 32,625 to Schwarz et al. teaches a method for the dynamic testing of electrical conductors by monitoring the change in resistance over an up and down ramped temperature.

U.S. Patent No. 4,792,683 to Chang et al. teaches a thermal technique for simultaneous testing of circuit board solder joints.

U.S. Patent No. 6,329,831 to Bui et al. teaches a method and apparatus for reliability testing of integrated circuit structures and devices.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone

numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
February 24, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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